Abstract of the Invention

A Viterbi decoder system is provided in accordance with the present invention. The decoder system includes a State Metric Update unit including a state metric memory and a cascaded Add/Compare/Select (ACS) unit. The cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory. An ACS stage is operable to identify a plurality of path decisions and path differences and communicate the identified path decisions and the identified path differences to a next ACS stage coupled thereto. The decoder also includes a Traceback unit for storing a set of accumulated path decisions in a traceback memory associated therewith, and performing a traceback on the set of accumulated path decisions. The path decisions associated with the ACS stage and the next ACS stage are accumulated as a set during the ACS operations before being written to the traceback memory, thereby minimizing accesses to the traceback memory. The path differences associated with the ACS stage and the next ACS stage provide a reliability estimation of the correctness of the path decisions.